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10/085,222	02/28/2002	David B. Kramer	9-22	6946

7590 02/28/2006

Ryan, Mason & Lewis, LLP  
90 Forest Avenue  
Locust Valley, NY 11560

EXAMINER
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TSEGAYE, SABA

ART UNIT	PAPER NUMBER
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2662

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/085,222

Applicant(s)

KRAMER ET AL.

Examiner

Saba Tsegaye

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04/22/02.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Specification***

1. The disclosure is objected to because of the following informalities: The attorney's docket number indicated on page 1, lines 6-12, should be deleted as it is not relevant to the application. See MPEP 608.01.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 20 and 21, recite the phrase "the maintenance" in lines 8, 6, and 6 respectively, and this phrase lacks antecedent basis.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for

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patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4-13, 15-18 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Fan et al. (US 6,389,019).

Regarding claim 1, 10, and 20, Fan discloses, in Figs. 2 and 3, a processor comprising: scheduling circuitry (6) for scheduling data blocks for transmission from a plurality of transmission elements (scheduling stream queues serving cells with different QoS within an ATM switch), the scheduling circuitry being configurable for utilization of at least one time slot table (5AB, to handle a large range of bit rates, a plurality of time wheels are employed with different time granularities) in scheduling the data blocks for transmission (scheduler unit selects a stream queue to be services, based on the queue information (abstract; column 6, lines 10-16); and

an interval computation element (a rate computation unit 8) associated with the scheduling circuitry (6) and operative to determine an interval for transmission of one or more data blocks associated with corresponding locations in the time slot table (the rate computation unit computes the rate for each stream queue that are assigned dynamically to the time wheels based on computed rate values), the transmission interval being adjustable under control of the interval computation element (column 3, lines 45-50) so as to facilitate the maintenance of a desired service level for one or more of the transmission elements (column 3, lines 30-64; column 18, line 38-column 19, line 5).

Regarding claim 4, Fan discloses the processor wherein the interval computation element is operative to determine periodically if the transmission interval requires adjustment in order to maintain the desired service level for one or more of the transmission elements (column 3, lines 45-66).

Regarding claim 5, Fan discloses the processor wherein the interval computation element makes a determination as to whether the transmission interval requires adjustment, after transmission of a specified number of the data blocks (column 16, lines 42-47).

Regarding claim 6, Fan discloses the processor wherein the interval computation element makes a determination as to whether the transmission interval requires adjustment, after transmission of each of the data blocks (column 5, lines 60-67).

Regarding claim 7, Fan discloses the processor wherein the transmission interval specifies a rate at which data blocks associated with corresponding locations in the time slot table are transmitted (column 3, lines 6-8).

Regarding claim 8, Fan discloses the processor wherein the interval computation element is operative to select the transmission interval from at least a first transmission interval associated with a first scheduling algorithm and a second transmission interval associated with a second scheduling algorithm (column 9, line 54-column 10 line 21).

Regarding claim 9, Fan discloses the processor wherein a given requesting transmission element is assigned to a location in the time slot table in accordance with the following equation:

$$\text{Assigned Time Slot} = \text{Current Time} + \text{Interval},$$

Where current time denotes a time corresponding to a current transmission time slot and Interval denotes the transmission interval (column 9, lines 1-2; column 7, lines 2-21).

Regarding claim 11, Fan discloses the processor further comprising traffic shaping circuitry (8) coupled to the scheduling circuitry (6), the traffic shaping circuitry comprising the interval computation element (column 6, lines 6-10).

Regarding claim 12, Fan discloses (Fig. 1) the processor further comprising transmit queue circuitry (2) coupled to the scheduling circuitry (3), wherein the transmission elements comprise one or more queues (1) associated with the transmit queue circuitry, the transmit queue circuitry supplying time slot requests from the transmission elements to the scheduling circuitry in accordance with the a traffic shaping requirement established by the traffic shaping circuitry (column 5, lines 5-45).

Regarding claim 13, Fan discloses the processor wherein the time slot table is stored at least in par in an internal memory of the processor (see fig. 2, 5A).

Regarding claim 15, Fan discloses the processor wherein one or more of the data blocks (data stream) (comprise data packets (data cells) (column 5, lines 45-49).

Regarding claim 16, Fan discloses the processor wherein the scheduling circuitry provides dynamic maintenance of the time slot table such that identifiers of requesting transmission elements are entered into the table locations on a demand bases (the time wheel structure is augmented with a plurality of priority levels (column 3, lines 1-9; column 18, lines 24-31)).

Regarding claim 17, Fan discloses wherein the identifiers of the transmission elements comprise a structure having one or more bits for allowing a given one of the transmission element identifiers to be linked to another r of the transmission element identifiers (column 11, lines 43-54).

Regarding claim 18, Fan discloses the processor wherein the processor configured to provide an interface for data block transfer between a network and a switch fabric (column 2, lines 41-43; column 6, lines 36-40).

6. Claims 1, 4, 14, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Boland et al. (US 5,889,763).

Regarding claims 1, 4 and 20, Boland discloses, in Fig. 1, a processor comprising:  
scheduling circuitry (12) for scheduling data blocks for transmission from a plurality of transmission elements (column 3, lines 17-21), the scheduling circuitry being configurable for

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utilization of at least one time slot table (100, 200) in scheduling the data blocks for transmission (column 5, lines 15-30); and

an interval computation element (scheduler 12 comprises a unit that calculates..) associated with the scheduling circuitry (12) and operative to determine an interval for transmission of one or more data blocks associated with corresponding locations in the time slot table (column 3, lines 21-27), the transmission interval being adjustable under control of the interval computation element (column 5, lines 25-30) so as to facilitate the maintenance of a desired service level for one or more of the transmission elements (column 5, lines 15-30; column 6, lines 9-25).

Regarding claim 14, Bolond discloses the processor (12) wherein the time slot table is stored at least in part in an external memory coupled to the processor (100, 200, see fig. 1).

Regarding claim 19, Bolond discloses the processor wherein the processor is configured as an integrated circuit (column 1, lines 4-7).

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 2 and 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al.



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Fan discloses all the claim limitation as stated above except for a machine-readable storage medium for use in conjunction with a processor.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use software-base machines, the benefit using machine-readable device is that programs can be changed and upgraded and new features are added easily than hardware changes.

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. in view of Pool et al. (US 5,455,948).

Fan discloses all the claim limitation as stated above; except for the interval computation element comprises a script processor.

Pool teaches a processor wherein priority computation element comprises of a script processor (fig. 3, the processor contains a script processor and scheduler for job queuing and scheduling and communicating with hosts, column 7, lines 6-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a script processor, such as suggested by Pool, in the rate computation unit of Fan in order to compute rate under software control. The benefit of software is that programs can be changed and upgraded and new features added easily than hardware changes.

10. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. in view of Boland et al. (US 5,889,763).

Fan discloses all the claim limitations as stated above except for the processor is configured as an integrated circuit.

Boland teaches a transfer rate controller that is configured as an integrated circuit (column 1, lines 4-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a processor in the form of an integrated circuit, such as suggested by Boland, in the system of Fan in order to minimize cost and space.

### *Conclusion*

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ono (US 6,667,977 B1) discloses ATM cell multiplexing apparatus and method.

Milliken et al. (US 6,526,062 B1) discloses system and method for scheduling and rescheduling the transmission of cell objects of different traffic types.

Airy et al. (US 2002/0159411 A1) discloses a method and system for scheduling the transmission of wireless data.

Gemar (US 6,414,963 B1) discloses apparatus and method for proving multiple and simultaneous quality of service connects in a tunnel mode.

Bonomi et al. (US 6,011,775) discloses method and apparatus for integrated traffic shaping in a packet-switched network.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saba Tsegaye whose telephone number is (571) 272-3091. The examiner can normally be reached on Monday-Friday (7:30-5:00), First Friday off.

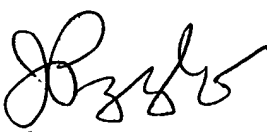
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ST

February 23, 2006



**JOHN PEZZLO**  
**PRIMARY EXAMINER**